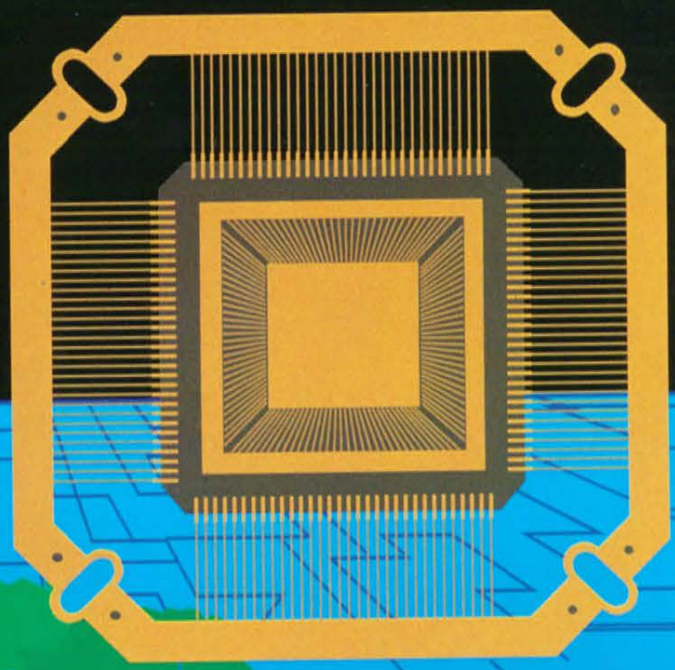
esa F-23
December 1989

# IRELAND
## - a new dimension -
# IN SPACE

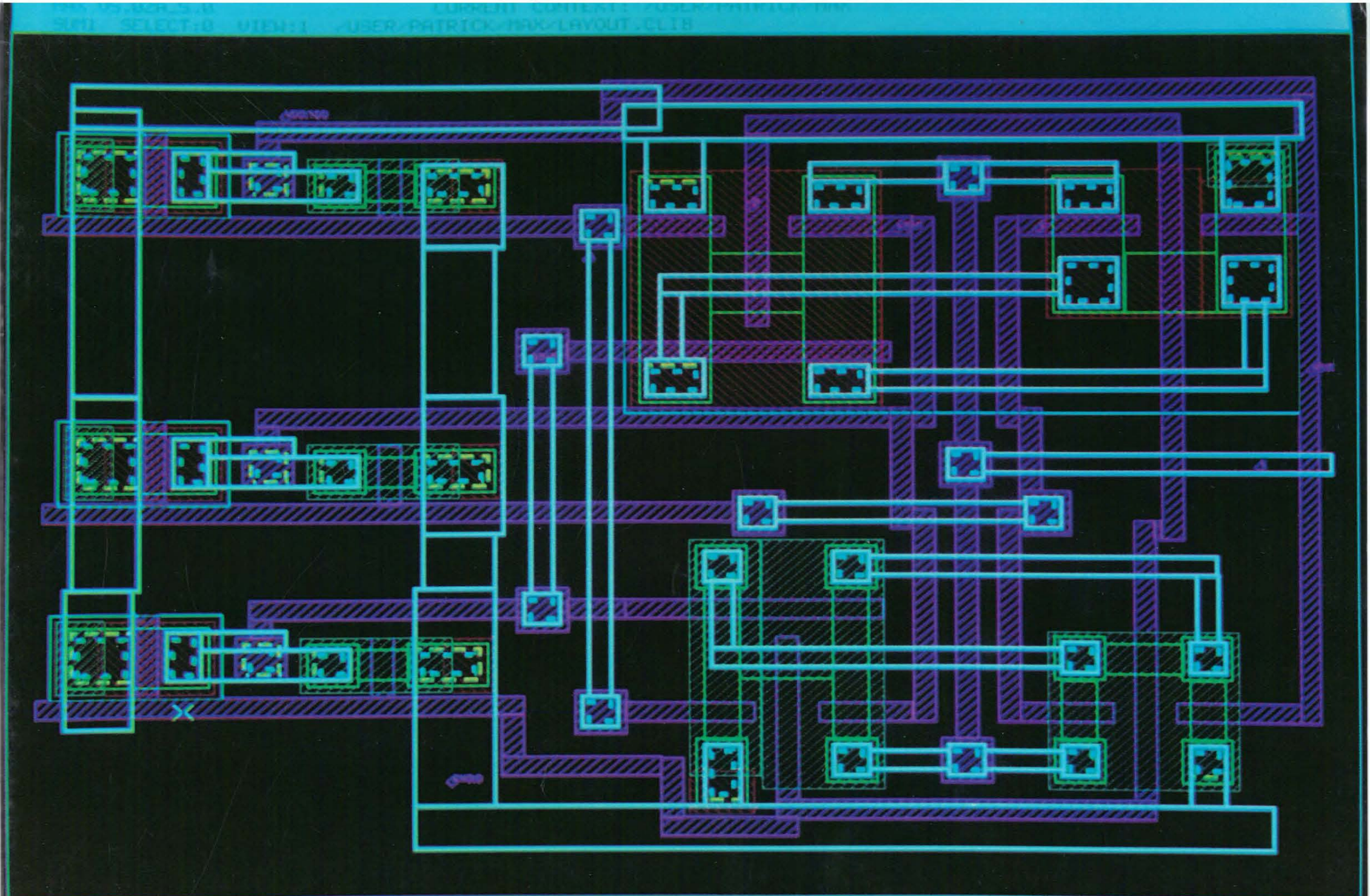


The Microelectronics Technology Support Laboratory -

Growing confidence in Ireland's hi-tech future

esa
european space agency

NMRC
IRELAND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The Interconnection and Packaging Group has worked closely with industry, particularly in the area of surface mount technology (SMT). As part of this interaction the group runs the secretariat for SMART (Surface Mount And Related Technologies) Group Ireland, and thus provides technical support to companies using advanced techniques for the production of electronic circuits. Another example of this interaction has involved the group in the production of prototype surface mount circuits for an Irish-based multinational company. This work involved the successful transfer of the production process to the company's manufacturing facility, which is currently used for series production.

**Question:** *Can any firm or industrial company call on the laboratory for help — and how can this best be done ?*

**Answer:** Thanks to the laboratory's close links with the European Space Agency's programmes, there is an excellent knowledge of both ongoing projects and future trends. Industrial companies in the space business, and those outside it, can make use of that expertise. The point is made that many industrial concerns outside the space sector have come to realise that the high standards demanded for space qualification can serve their purposes as well, saving much time and effort on research.

For more details of NMRC/MTSL please contact:

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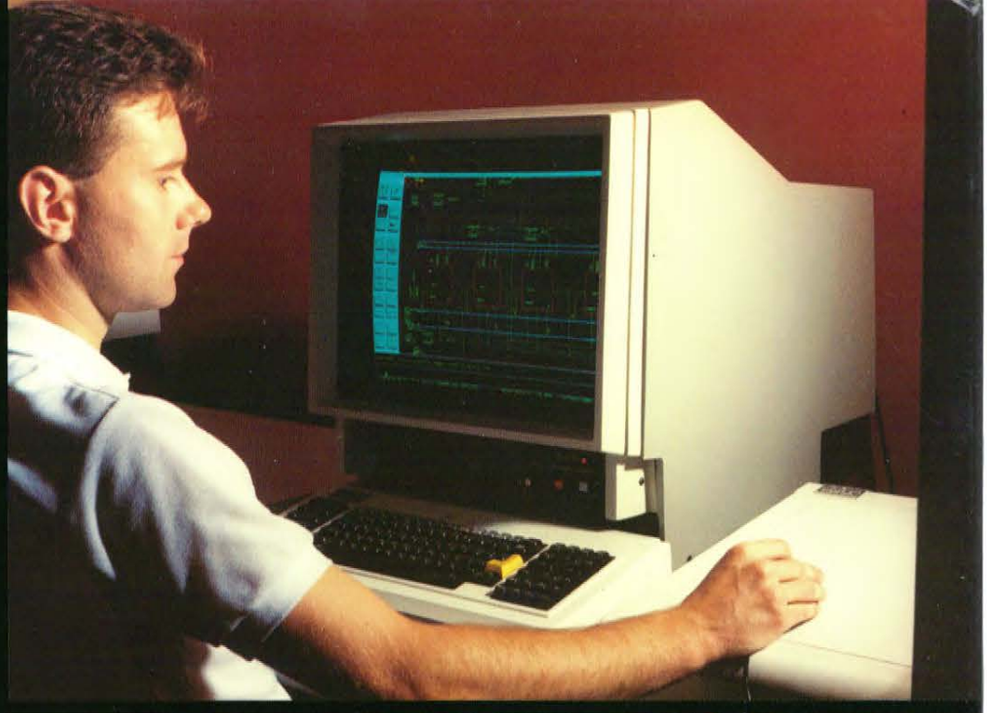
Cork,
Ireland

*The work carried out in this laboratory will be to a world class standard and is at the leading edge of today's microelectonic technology*



**Question:** *What is the Microelectronics Technology Support Laboratory?*

**Answer:** The short answer is — the Irish National Microelectronics Research Centre (NMRC) in Cork under another name.

Going back a short time, the European Space Agency (ESA) was looking for a laboratory which could provide long-term technological support, basic studies, and related activities to the Agency's space programmes in the disciplines of semiconductors, covering in particular microwave, optoelectronic, power, analog and digital functions.

The Irish NMRC was already making a name for itself in support of industrial developments in microelectronics, and ESA quickly recognised that such expertise and dynamic interaction with the customer could be geared to assist the European Space Industry in critical areas.

The MTSL is able to call on all staff and all research taking place at NMRC in its support of European Space activities.

**Question:** *What were the specific advantages in choosing Cork for this advanced, innovative Centre?*

**Answer:** A strong research base was needed if Ireland wanted to enjoy success in some specialised 'hi-tech' discipline. The Irish government recognised that the microelectronics research being done in University College Cork not only fitted the bill but was ready to expand to meet industry's wishes for practical technological support. The growth in all senses of NMRC since its formal inauguration in 1981 has fully justified the government's confidence. The fact that ESA then chose NMRC to set up the Microelectronics Technology Support Laboratory further endorses the decision.

*This new facility represents a major opportunity for Cork, and indeed for Ireland to increase its involvement in the highly specialised and rapidly expanding area of space technology.*

**Question:** *What specific expertise and facilities does NMRC/MTSL have to offer?*

**Answer:** The individual sheets in this folder are devoted to answering this question in some detail, but essentially the customer is offered the facilities of a silicon fabrication laboratory, the III-V laboratory which specialises in the use of non-silicon elements in microelectronics, a computer-aided design and mask making department, a packaging and interconnection group, and a specialised test support laboratory.

MTSL can offer:
- component selection evaluation and qualification,
- independent assessment of products, with emphasis on suitability for use in space projects,
- facilities to assess component development, and new concepts,
- a failure-analysis service,
- a consultancy service at all stages of projects.

*The NMRC's vast experience is the base on which Ireland's ESA laboratory will build.*

**Question:** *What has been achieved by NMRC for industry to support the confidence in its future role, especially as MTSL?*

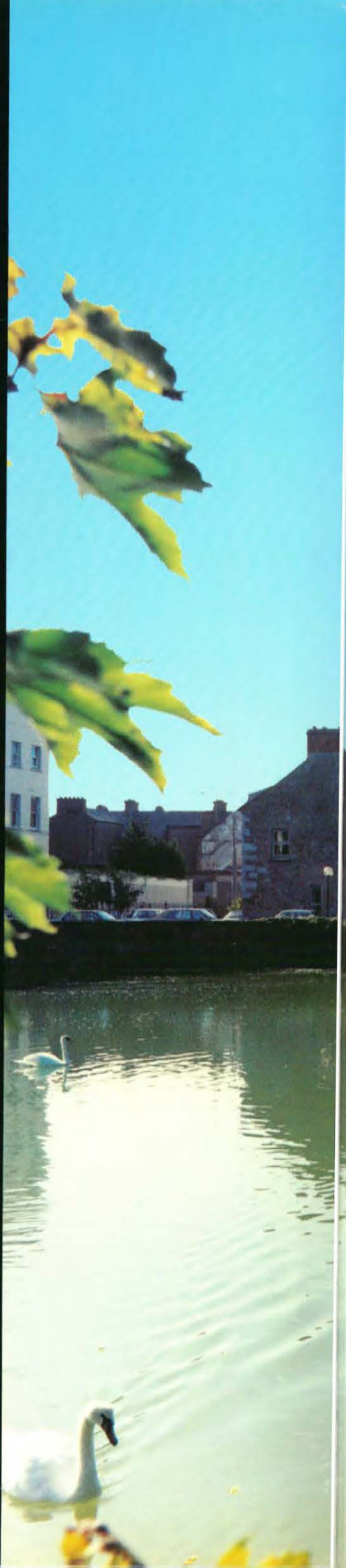
**Answer:** Support to industry in Ireland was one of the primary reasons for establishing the NMRC. The Centre specialises in four main areas of technology: silicon fabrication, CAD, III-V compounds, and interconnection and packaging.

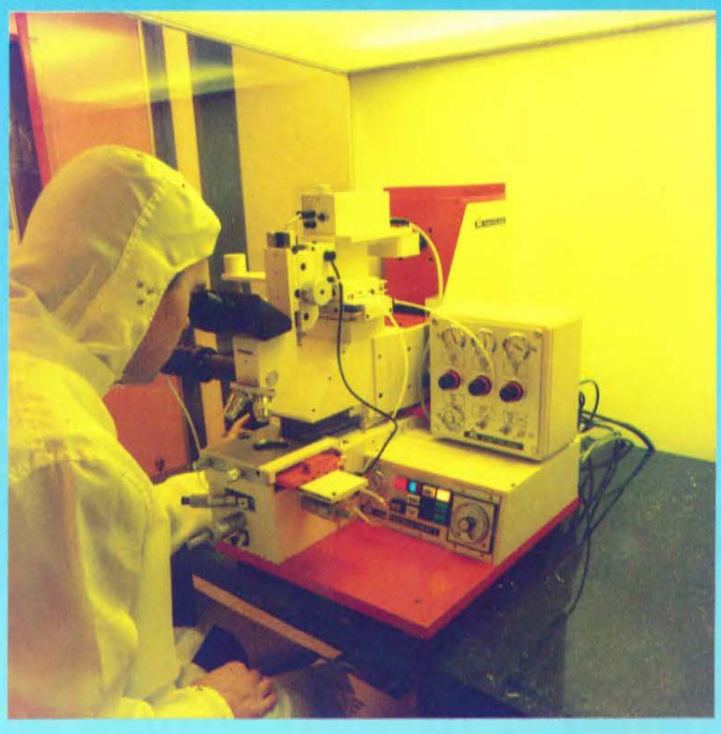
Since the opening of the Centre, technology in all these areas has contributed significantly to industrial development through healthy interaction between the Centre and industry both in Ireland and abroad. The Centre is involved in 18 ESPRIT and RACE projects, providing work in all four areas.

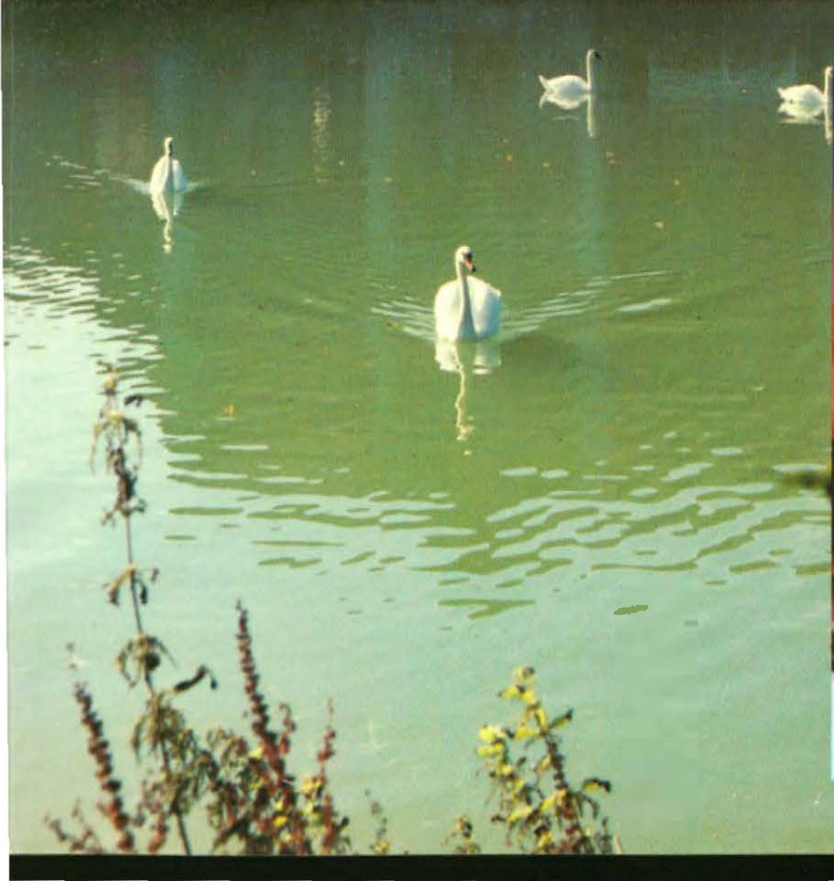
Those in which the Silicon Group is involved cover the spectrum from the evaluation of material techniques and advanced packages to smart power devices and the development of small geometry technology for analogue circuits and non-volatile memory applications.

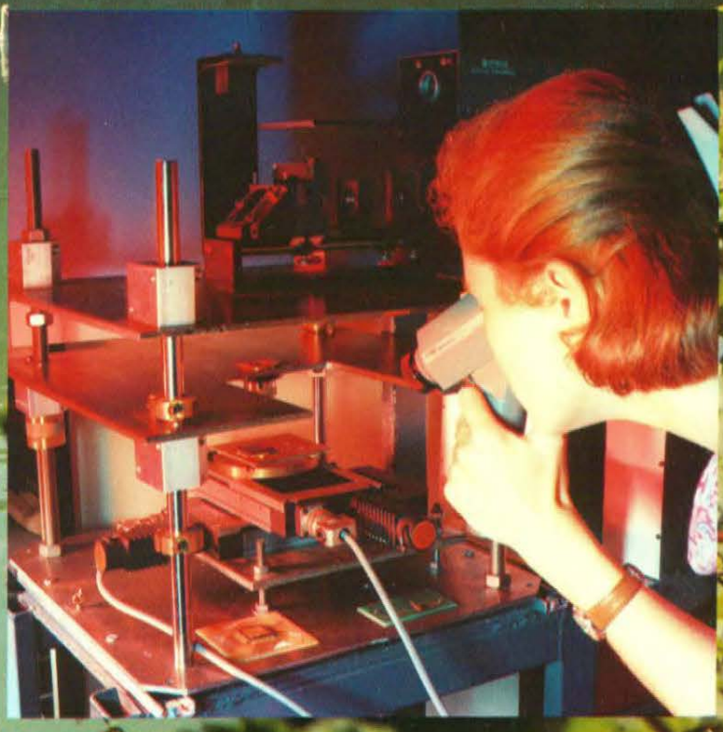
The CAD Group promoted the use of ASICs in Irish industry through the provision of courses and a design service. Circuit simulation software, and device and process modelling software has also been successfully developed, and is now being used by European industry.

The III-V laboratory successfully developed new products including a high quality electron sensitive resist for an industrial company. This resist was demonstrated by the fabrication of state-of-the-art sub-micron gate GaAs MESFETs.









# The III-V Laboratory

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Friendly competition can provide considerable stimulus, and this is true of the III-V laboratory within NMRC. The team members are enthusiastic in outlining the advantages of Gallium Arsenide (GaAs) and other III-V compounds:

- higher electronic mobility, making it suitable for high frequency devices, (mixer diodes, MESFETs),
- larger band gap than silicon, resulting in a higher maximum operating temperature, (200 vs 125°C),
- direct bandgap, making it suitable for opto-electronic devices, (LED's etc.).

In addition there is the fact that they have better resistance to ionising radiation.

Team members are also quick to point out that disadvantages, at the moment, are higher costs and lower processing yields.

ESA is very interested in possible developments in this subject, and has called upon the laboratory to review activities in Europe in III-V group technology; the review to cover microwave and millimetric wave devices and integrated circuits. In this way existing industrial ability can be measured against ESA's stated requirements, and work programmes can be initiated.

*Plasma glow surface cleaning to prepare GaAs surface for metallisation.*


*Electron beam evaporator to deposit metallic Schottky contact.*

ESA also has a need for highly sensitive GaAs diodes for the far-infrared and radio-astronomy missions it is planning. Current technology cannot meet the requirements, so the laboratory has a work programme for the:

- development and utilisation of techniques for sub-micron geometries (to yield below 1 fF capacitance diodes and few ohm resistance),
- improvement in diode reliability and power handling,
- achieving of the Shot noise limit in sub-millimeter mixers,
- testing of diodes (lifetime, RF characteristics).

Optical space communication systems will call for high power laser diodes. The design of such diodes is undergoing a rapid evolution, and additional knowledge is needed about their lifetime under special conditions of modulation, power, and environment. The laboratory is undertaking a programme to assess metallisation and reliability of laser diodes.

At the same time the laboratory is playing a significant role in new projects covering:

- semi-conducting optoelectronic devices,
- III-V quantum well structures,
- basic research into quantum effects in lateral microstructures,
- INGaAs JFET simulation,
- dry processable resists for GaAs,
- optical waveguides,
- nonlinear organic polymers

To carry out its role the laboratory has equipment and facilities necessary to fabricate III-V IC chips and devices at an R&D level, including:

- an MRC triple-target radio-frequency sputtering system,
- a variety of plasma etch systems,
- an electron beam and vacuum evaporator,
- near and deep UV Karl Suss contact aligners,
- a Tempress scriber,
- a Tempress dicing saw,
- a Polaron profile plotter,
- a Logitech crystal polisher,
- an MOCVD materials growth system,
- an Electron Beam Lithography system.
- an ion/radical beam etch/deposition system

*Photolithographic patterning of III-V wafers using the near and deep-UV mask aligners*

# Silicon Fabrication Laboratory

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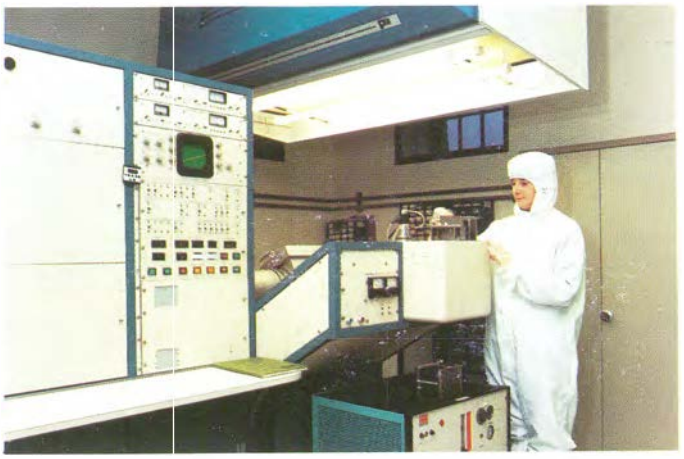
The silicon fabrication laboratory offers comprehensive services to industry seeking help in the fabrication sequences used in today's integrated circuits.

The laboratory is one of the main elements of the Centre, with more than 4.000 sq.ft. of better than class 10 000 space housing the equipment. Two attached class 100 yellow rooms contain the photolithography process.

Ten Tempress built diffusion/oxidation tubes with pyrogenic (burnt $H_2$) oxide and liquid or solid source diffusion capabilities are the mainstay of the laboratory equipment. Dedicated wet stations in class 100 benches provide the other basic processing equipment. Main items of an advanced nature include:

- an Eaton 200 keV medium current ion implanter equipped with gaseous (B, As, P) and solid (other) sources available for threshold shifting and general doping tasks,
- two Tempress low pressure chemical vapour systems providing silicon nitride and polysilicon deposition capability,
- an atmospheric deposition reactor can deposit doped or undoped oxide; while a plasma-enhanced chemical vapour deposition system also allows deposit of undoped oxides and nitride,
- an upgraded Balzers magnetron sputtering system capable of sputtering from three targets, and equipped with a radio frequency etch is used for metallisation tasks,
- plasma etching equipment for polysilicon, nitride, oxide and aluminium; a new oxide etcher with submicron capability was acquired in 1989.



*Loading wafers into the ion-implanter*


*Unloading the Balzers metalisation sputtering system*
*Below: General view of the silicon fabrication laboratory: staff at (left to right) furnaces, spin-dryer, wet benches*

With such facilities the laboratory can offer a precision-based service to both space and non-space oriented industry. The photolithographic process is positive resist based, and the equipment includes:

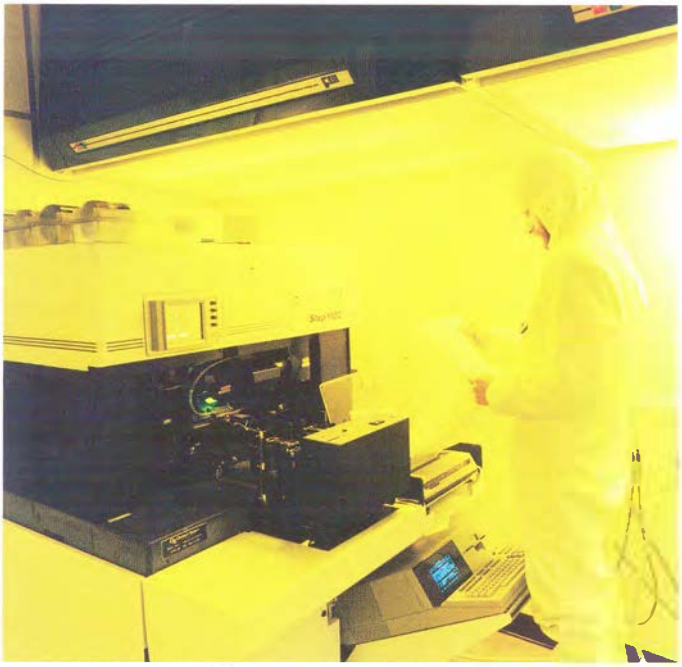
- an Eaton coater developer system for positive resist processing and baking,
- a Canon mask aligner,
- an Ultratec Stepper for 3 $\mu$m to 0.8 $\mu$m fine line lithography.

The role of the Silicon Fabrication Laboratory within MTSL is initially tied to the development of radiation dosimeters. Against the background of work already done in this subject, ESA has asked for more detailed investigation into:

- characterising thicker gate oxides,
- the effects of implanting the channel regions to reduce the threshold voltages close to zero.

Special emphasis is being placed on incorporating compensation for the temperature coefficient of threshold voltage.

*Taking line-width measurements using Vickers Image Shearing system*



*Ultrastep 1100 Direct Step-on Wafer (DWS) lithography system*

*At the wet bench: checking that the etch is complete*

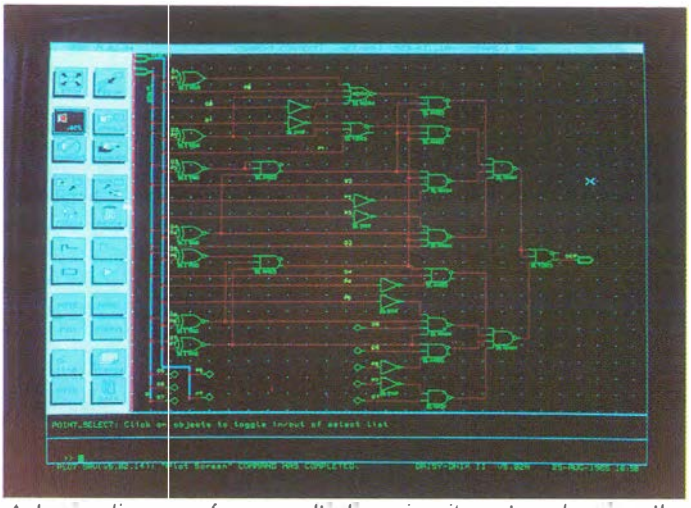
# Computer Aided Design



It is a modern axiom that behind every successful design engineer there stands a good computer-aided-design (CAD) group. This is certainly true for NMRC/MTSL.

The increasing complexity of integrated circuits and the requirement for submicron sized dimensions could not be sustained were it not for the tools which the multi-processor CAD department offers towards the creation of masks intended for integrated circuit fabrication by means of optical and electron-beam lithography.

The complexity of a large integrated circuit forces engineers to adopt a structured, top down design methodology. At the top of the hierarchy are abstract functional descriptions of the intended behaviour of the circuit. The lower levels have more detailed, less abstract views of the circuit with the lowest level comprising the geometrical layout of the masks. The NMRC's CAD facilities



*A logic diagram for a multiplier circuit, entered using the schematic capture program.*

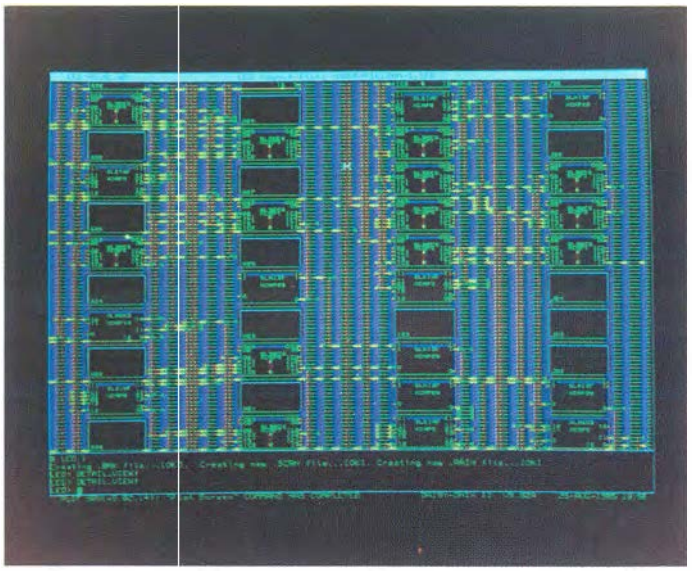
*Integrated Circuit designers using the design workstations*

are focused on this top down methodology, providing the designer with tools for documenting, analysing and checking the design at each level.

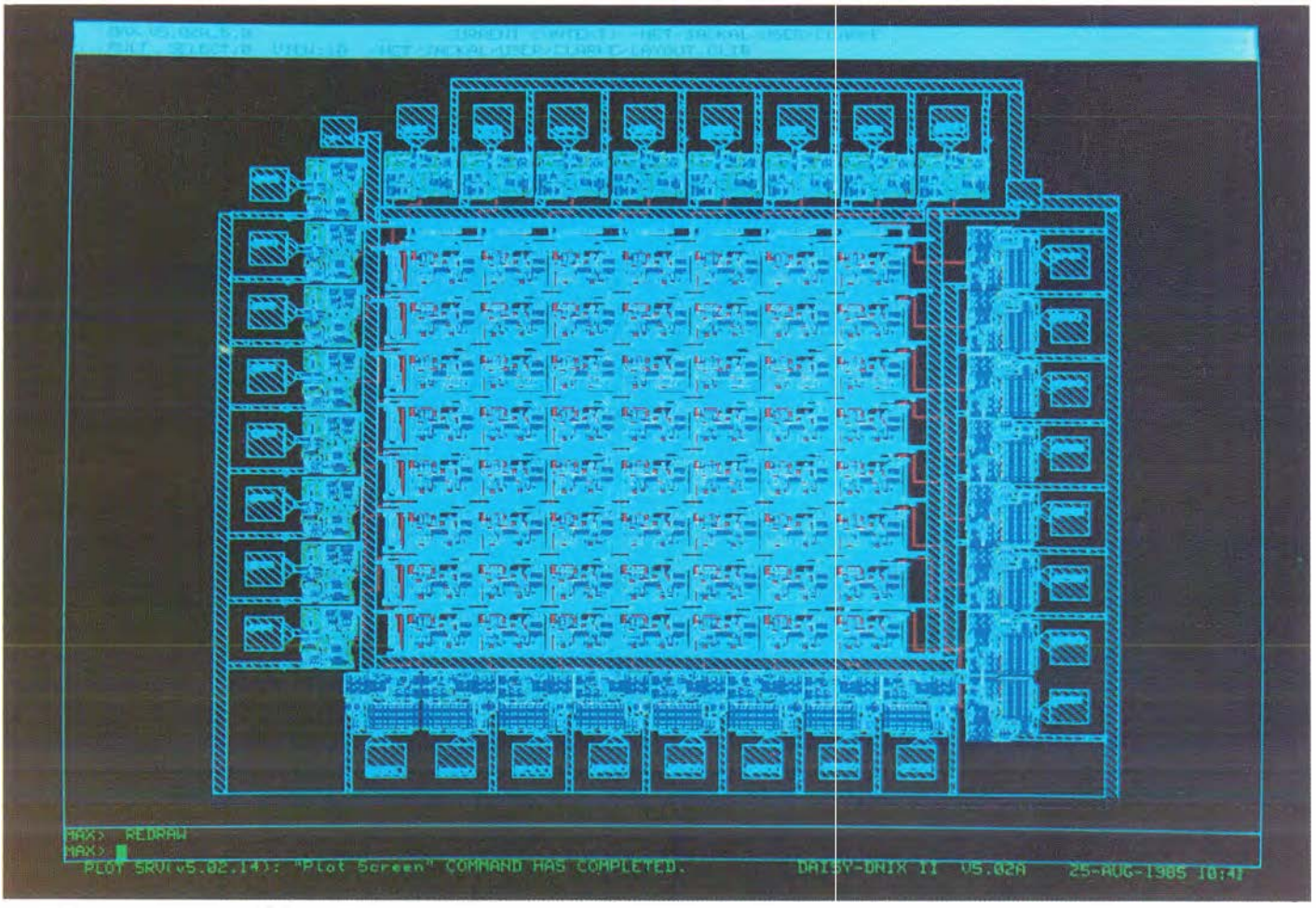
The CAD equipment consists of Mentor Graphics and DAISY workstations, supported by a range of DEC and Sun workstations for more general computing. Both Mentor and Daisy workstations provide schematic capture for design entry, with behavioural and logic simulation for the higher levels of design. Gate array and standard cell block placement and routing programs are supported. These automate the conversion of netlist descriptions of application-specific integrated circuits into the geometric layouts required for mask making.

The simulation of transistor level design is supported by SPICE, from the University of California at Berkeley, SIMON a fast timing simulator from Cadence, and SUGAR, a fast mixed analog digital simulator developed in NMRC. The entry of IC layouts is based on the Mentor Graphics' Chipgraph. This is complemented by a design rule checker and circuit extractor which produces SPICE readable files from the layout. Hardcopies of the layouts are available on a Versatec raster plotter. Interfaces to the in-house David Mann Pattern Generator and an electron-beam lithography machine are supported.

The CAD group also provides support for process development. By simulating a proposed semiconductor device before fabrication, process engineers can minimise the number of expensive and time consuming experimental iterations required to optimise its performance. A number of simulators are supported, including MINIMOS from the Technical University Vienna, HFIELDS from the University of Bologna, and an internally developed program for GaAs and GaInAs transistors.



*Detail of a CMOS Gate Array which has been automatically placed and routed on the DAISY workstation.*




*Overview of the completed layout of a multiplier design.*

# Interconnection and Packaging Laboratory

ESA F-23 insert
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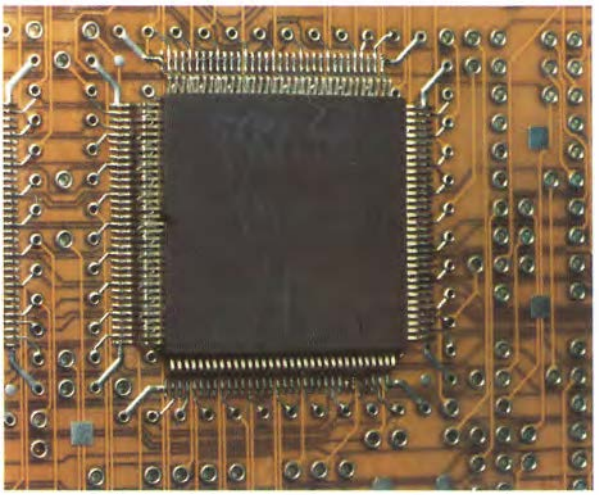
The rapid evolution of microelectronics design and fabrication technology in recent years has lead to the development of highly complex silicon and compound semiconductor integrated circuits. These developments have resulted in integrated circuits with:

- die sizes of 1 $cm^2$ and greater
- pincounts of 300 and higher
- power densities of up to 50 watts per $cm^2$
- signal speeds requiring transmission line interconnection

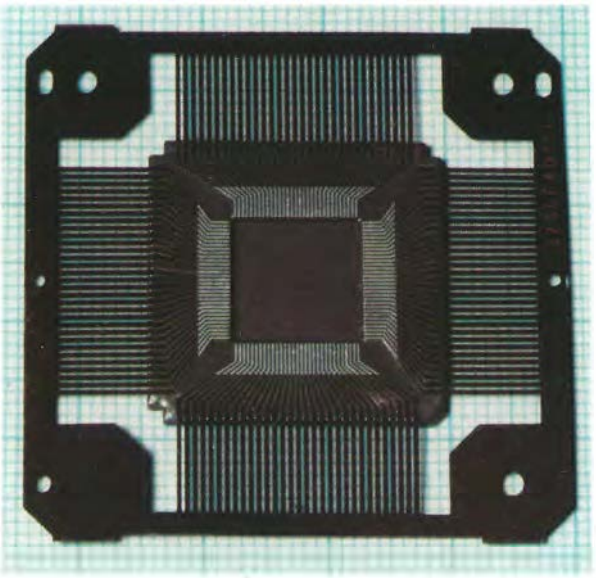
It has become increasingly obvious that advances in the methods and materials used for packaging and assembly of these highly complex circuits have not kept pace with integrated circuit development. Advanced integration technology has meant that the relative cost of integrated circuits has fallen and semiconductor devices often now represent less than 10% of the overall equipment costs. Integrated circuit performance and operating speeds have also improved, and consequently, the limitations of conventional packaging and interconnection technology have become more pronounced, leading to a worldwide search for techniques suitable for use in the next generation of electronic equipment.

The Interconnection and Packaging Laboratory is addressing many aspects of IC packaging technology, including the development of high density interconnection substrate technology and the examination of the reliability of new generations of IC packages. The laboratory was initially set up as a facility capable of research and prototyping in the area of Thick Film Hybrid Circuits and this activity remains part of the work of the laboratory. Since 1983, it has been involved in advanced IC packaging through the ESPRIT (European Strategic Programme of Research and Development in Information Technology) programme with work in three projects in the first phase of the programme: MR-10-MOV (High Pin Count IC Packaging), ESPRIT 544 (High Density Interconnect) and ESPRIT 824 (Wafer Scale Integration). In MR-10-MOV, the laboratory worked on the development of special purpose integrated circuits to evaluate the reliability of IC packages and this work was continued after the completion of MR-10-MOV to produce further generations of these ICs which are now available for use by industry. In ESPRIT 544 and 824, the laboratory was involved in development of techniques for very high definition electroplating of interconnects both on ceramic and silicon. ESPRIT 544 also involved work with Tape Automated Bonding (TAB) and flip-chip IC attachment techniques.

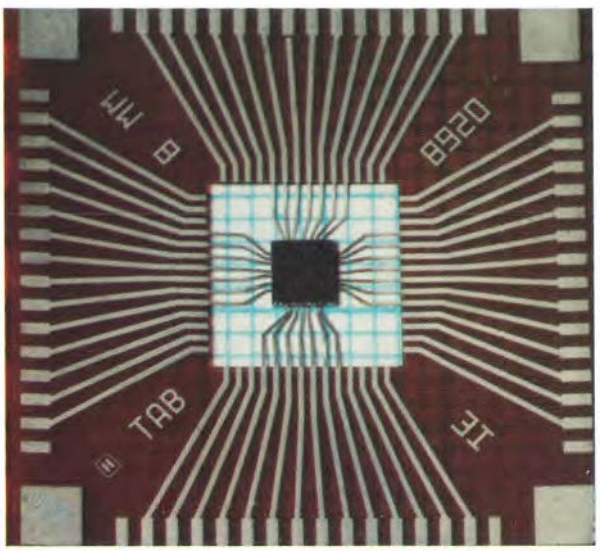
The laboratory currently has two senior research scientists, two research engineers, three technicians, and three postgraduate students.



*132 lead plastic quad flat pack (PQFP) surface mounted on high density printed circuit*



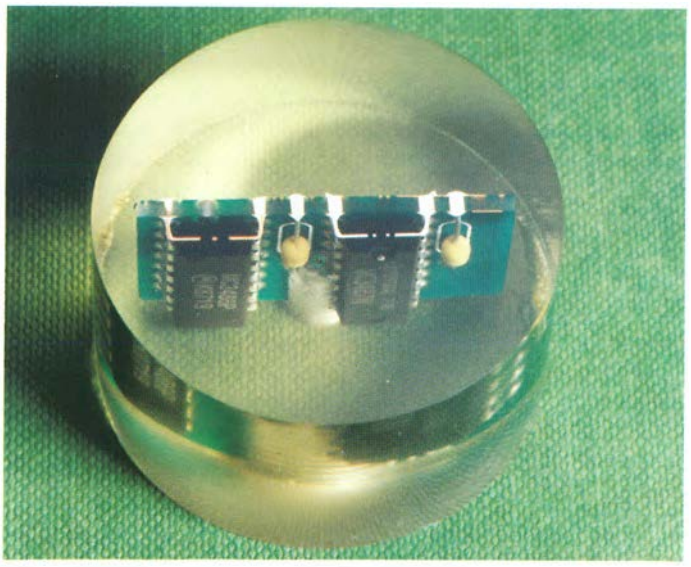
*124 lead CERQUAD high pincount glass sealed ceramic chip carrier*




*28 lead chip inner-lead bonded on TAB (Tape Automated Bonding) tape. TAB is a very high density chip packaging technique.*

In 1988, the Group became involved in ESPRIT II within project 2075 (APACHIP - Advanced Packaging for High Performance) in which it is supplying IC package thermal test chips to project partners and is also investigating the application of scanning acoustic microscopy to the non-destructive imaging of surface and sub-surface defects in advanced packaging materials and structures.

As part of the establishment, by the European Space Agency (ESA), of a Microelectronic Technology Support Laboratory at NMRC, the laboratory is in the process of establishing facilities for IC packaging and environmental testing to MIL. STD. 883C. The packaging facility will consist of equipment for die attach, gold and aluminium wire bonding, package sealing, fine and gross leak testing and IC package assembly. The environmental facility will include equipment for thermal shock, temperature cycling, temperature/humidity testing as well as computerised data acquisition systems.



*Metalographic microsection through IC package soldered to printed circuit board.*

*Loading of test specimens into environmental test chamber prior to performance of temperature cycling tests*

Under this contract, the Group will undertake the evaluation of high pin-count packaging and interconnection technologies expected to be used in future ESA projects. The evaluation will cover such topics as visual inspection criteria, reliability for both ceramic pin grids arrays (PGAs) and fine pitch chip carriers, assembly of fine pitch packages and evaluation of advanced substrate technologies. IC package assembly for fine pitch packages and tape automated bonding (TAB) is also being investigated as part of an EOLAS project on laser soldering.

The Group is also active in providing technical support to industry in the form of consultancy, access to technical literature and electronic product databases, prototyping (surface mount circuits, packaging for ASICs and is in the process of establishing a CAD facility for PCB layout) and services (SEM, crosssectioning, failure analysis etc.). As part of this function the laboratory also runs the secretariat for SMART Group – Ireland, a technical support group to companies involved in surface mount and related technologies. The Group has now more than 55 members and organises regular workshops and seminars for its members.


*Detail of output from thermal modelling software in use in the laboratory.*

*System for automatic thermal characterisation of IC packages*

# Integrated Circuit Test Engineering Laboratory

ESA F-23 insert
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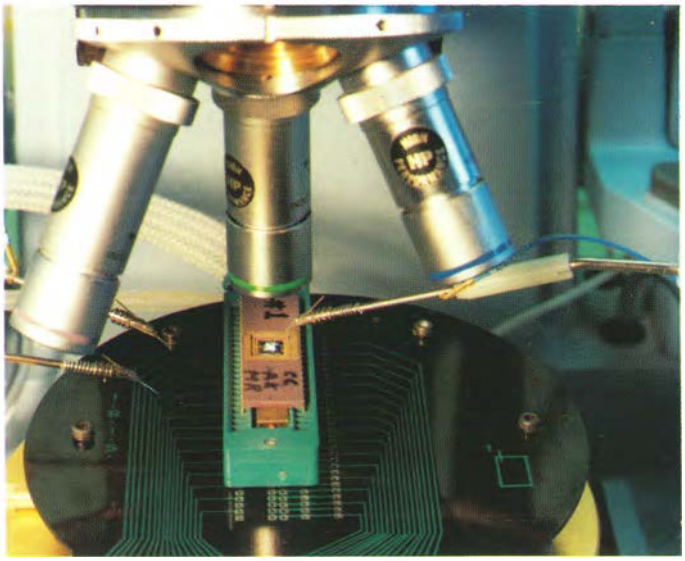
The subtitle for this section could be 'looking for the ID of the IC', for the tasks of the laboratory are not unlike those of the psychoanalyst probing into human characteristics.

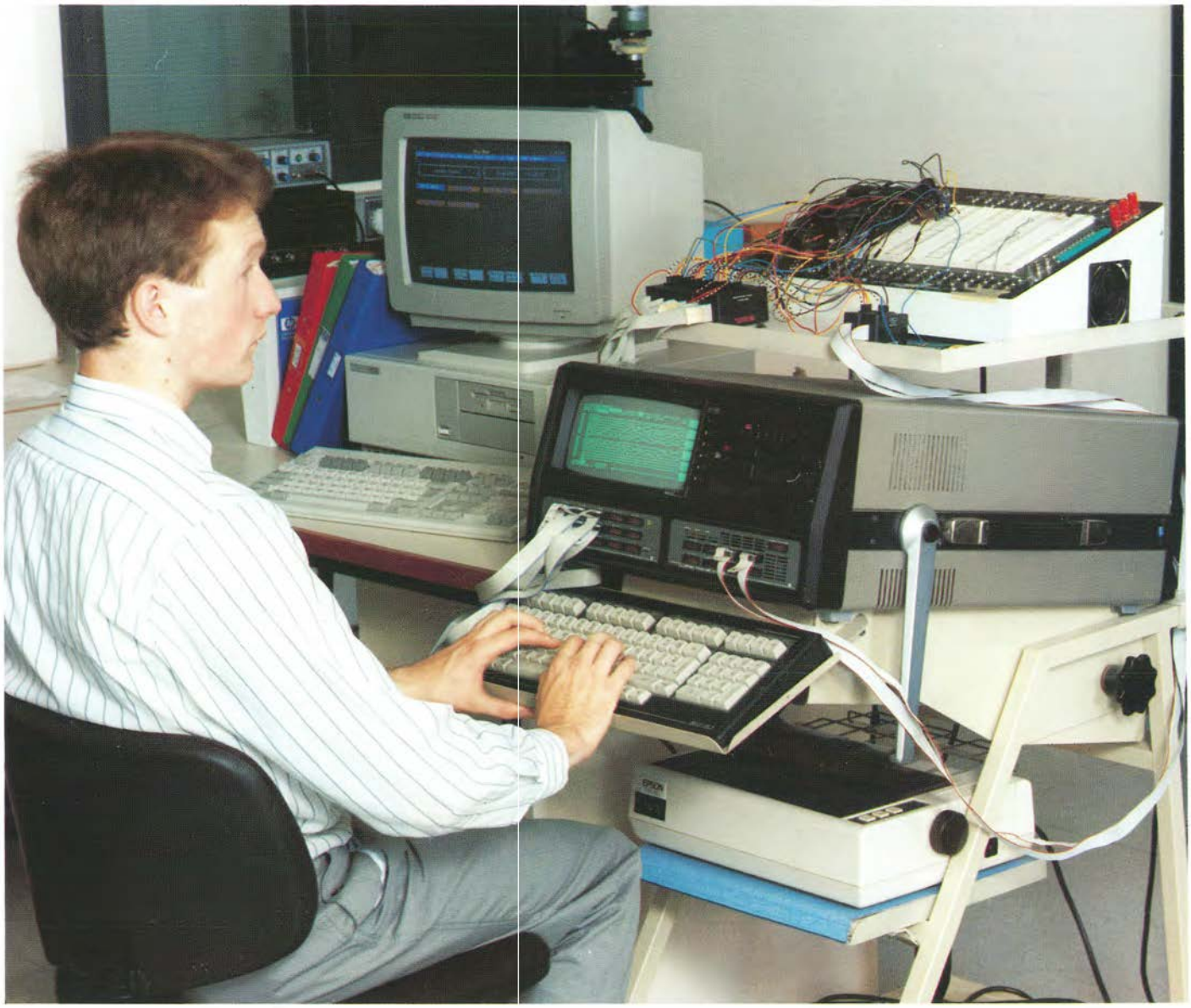
When ICs which have failed in operation are sent to the laboratory to find out cause and effect, the laboratory staff call upon all analytical tools to probe whether the fault lies in the processing, design, or misapplication of the IC.

Understanding how products should work is essential before an indepth understanding of how products have failed can be reached. Integrated circuit failures may occur during processing, electrical test, packaging, reliability testing, transportation, storage or use.

Failures which occur during processing, electrical test or packaging reduce overall yield for a manufacturer, while failures which occur during reliability testing, transportation, or in normal use call into question the reliability of the product.



*Electrical analysis of internal circuitry using sub-micron flying probe.*



*Digital IC fault verification using computer-controlled Atlas test system.*

It is at this point that ESA's interest in the laboratory comes into focus. High reliability of microelectronic components is crucial for space applications, so microelectronic products proposed for use in space projects must be thoroughly tested in a simulated space environment. When IC failures do occur during such tests (ie. anomalous operation, persistant malfunction or radiation induced malfunction) it is essential to be able to identify the cause of failure. Also, whether or not failures occur, it is equally as important to be able to analyse the design and processing methodology employed in the manufacture of these IC's. Such analysis can reveal the strengths and detect any weaknesses in the manufacturing process in the context of space applications. ESA looks to MTSL to provide the facility and expertise to address these analytical requirements.

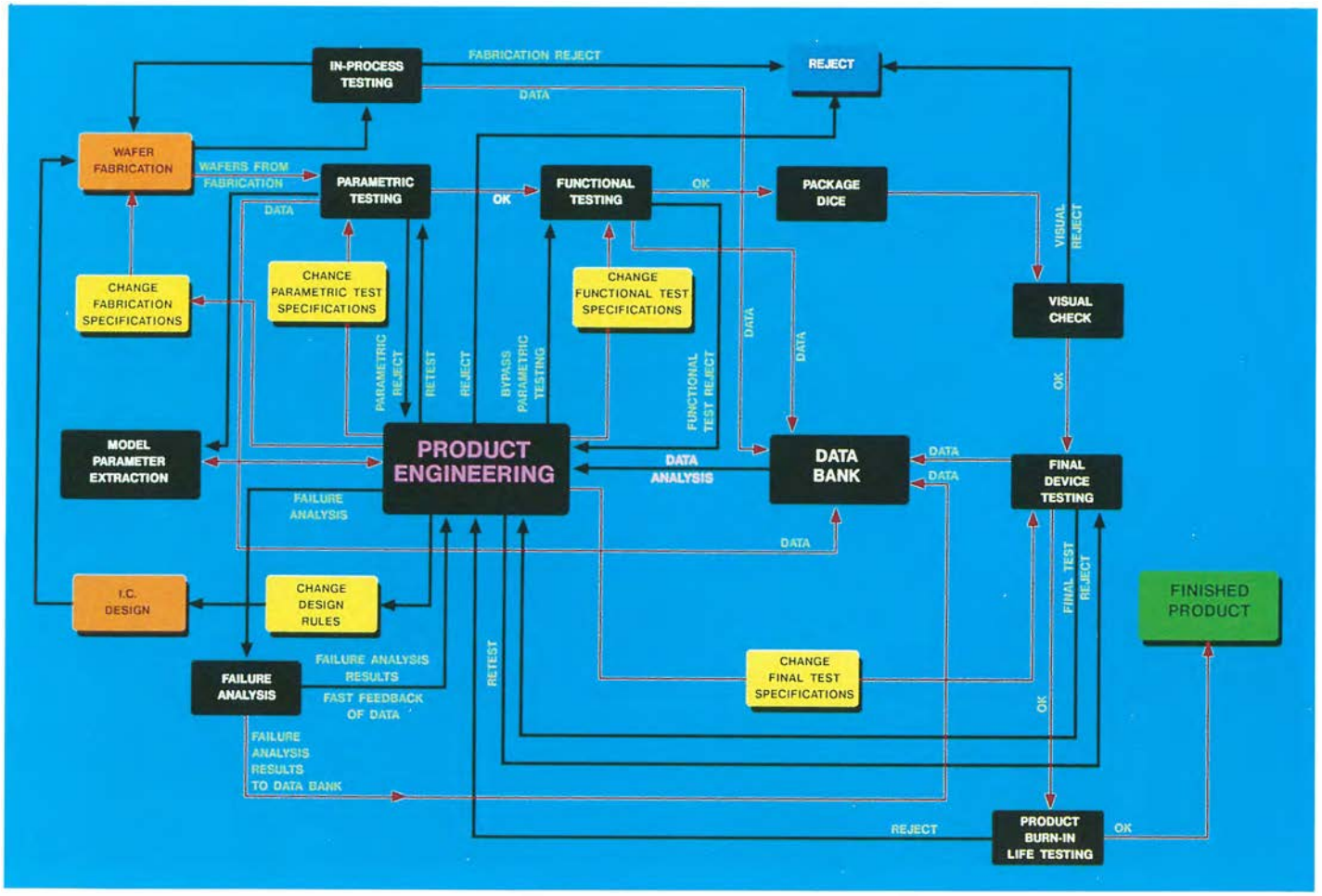
Within the context of MTSL the role of the IC Test Engineering laboratory is centred on the following eight activities in support of the European Space venture:

a. assessment of IC failure mechanisms.
b. investigations of reliability improvements of advanced/new processes.
c. analysis of destructive and reliability effects on microcircuits.
d. qualification of microcircuits for space applications.
e. assessment of new processes.
f. reverse engineering of microcircuits.
g. development, assessment and characterisation of advanced techniques for IC failure analysis.

When the cause of a failure is not readily accessible, it is necessary to perform IC failure analysis and reverse engineering. These activities require an indepth study of the IC manufacturing process of complex IC's such as large memories and microprocessors. IC failure analysis and reverse engineering is a highly methodical process in itself. Great care must be taken to extract as much information as possible at each analytical step. This is important because

the analysis procedure involves a step by step destruction of the IC. A wide knowledge base of various design and processing techniques is essential to do such analysis, as well as the availability of a wide range of analytical equipment such as electron, acoustic and optical microscopy, probing, electrical test and materials analysis equipment.

In summary, the main activities within this laboratory are in:
- process characterisation,
- process monitoring,
- circuit characterisation,
- materials characterisation,
- IC failure analysis and
- reverse engineering.



The laboratory offers comprehensive support for the processing and design activities of the Centre, as well as providing a service to industry in specialised areas of characterisation and analysis. The primary equipment resources of this laboratory are:

- Keithley S350 parametric test system.
- HP-4062UX process characterisation system.
- High voltage DC characterisation system.
- Spreading Resistance profiling system.
- Network / Spectrum / Impedance analysis system.
- CV / CT and Electrometer measurement.
- Liquid Crystal Microthermography system.
- Decapsulation, Crossectioning, Delineation, Delayering, Lapping & Staining.
- Optical / Electron / Acoustic microscopy.
- Analytical probing.
- Thermal wave analysis system.
- Digital IC verification system.

*Liquid crystal microthermography - analysis of failed integrated circuits*


*Semi-automatic spreading resistance profiling system for extracting carrier concentration profiles of diffused regions*

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**Lee Maltings** the home of NMRC has a colourful and long history. The original lease in 1796 put the yearly rent at £25 plus thirty good salmon (which explains the salmon weather-vane). Before 1800 a bolting mill and a brewery had been built on the land. In the 19th century more buildings were added, and part of the stream was later filled in. Today's NMRC buildings can be traced to Lee Mills (formerly Hayes' Mills), built 1796/1798, to which a wing was added in 1902/1903, and River Lee Porter Brewery, built in 1796/1798. Truly an example of modern technology making use of traditional values.